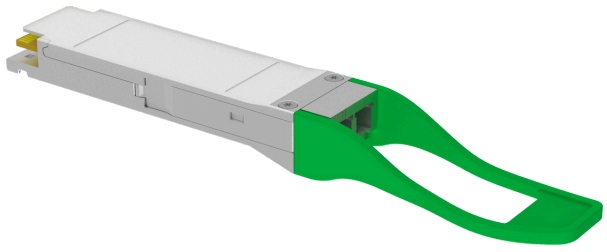
QSFP28 100GBASE CWDM4 2km Optical Transceiver

Features

- Hot-pluggable QSFP28 form factor
- 4 channels full-duplex transceiver module
- Supports 103.125Gb/s aggregate bit rate
- 4 channels DFB-based CWDM uncooled transmitter
- 4 channels PIN ROSA
- Internal CDR circuits on both receiver and transmitter channels
- 3.5W maximum power dissipation
- Maximum link length of 2km on SMF with KR4 FEC
- Duplex LC receptacle
- Operating case temperature range: 0 to 70°C
- Single 3.3V power supply
- RoHS-6 compliant (lead free)



Applications

- 100GE CWDM4 applications with FEC

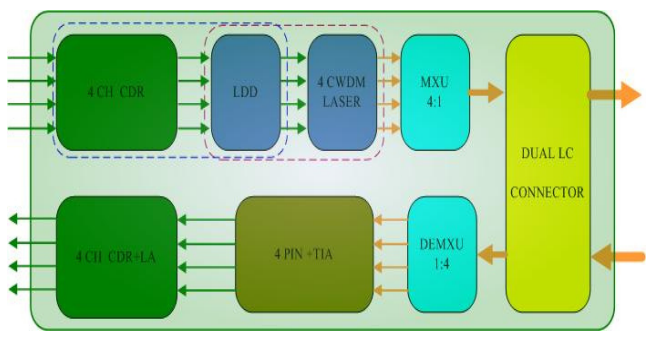


Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbo l	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Ts	-20	85	ºC
Case Operating Temperature	Tc	0	70	ºC
Humidity (non-condensing)	Rh	5	85	%
Damage Threshold (each lane)	THd	5.5		dBm

Recommended Operating Conditions

Parameter	Symbo l	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tc	0		70	ºC
Data Rate Per Lane	fd		25.7812 5		Gb/s
Humidity	Rh	5		85	%
Power Dissipation	Pm			3.5	W
Link Distance with G.652	D			2	km
		0.002			

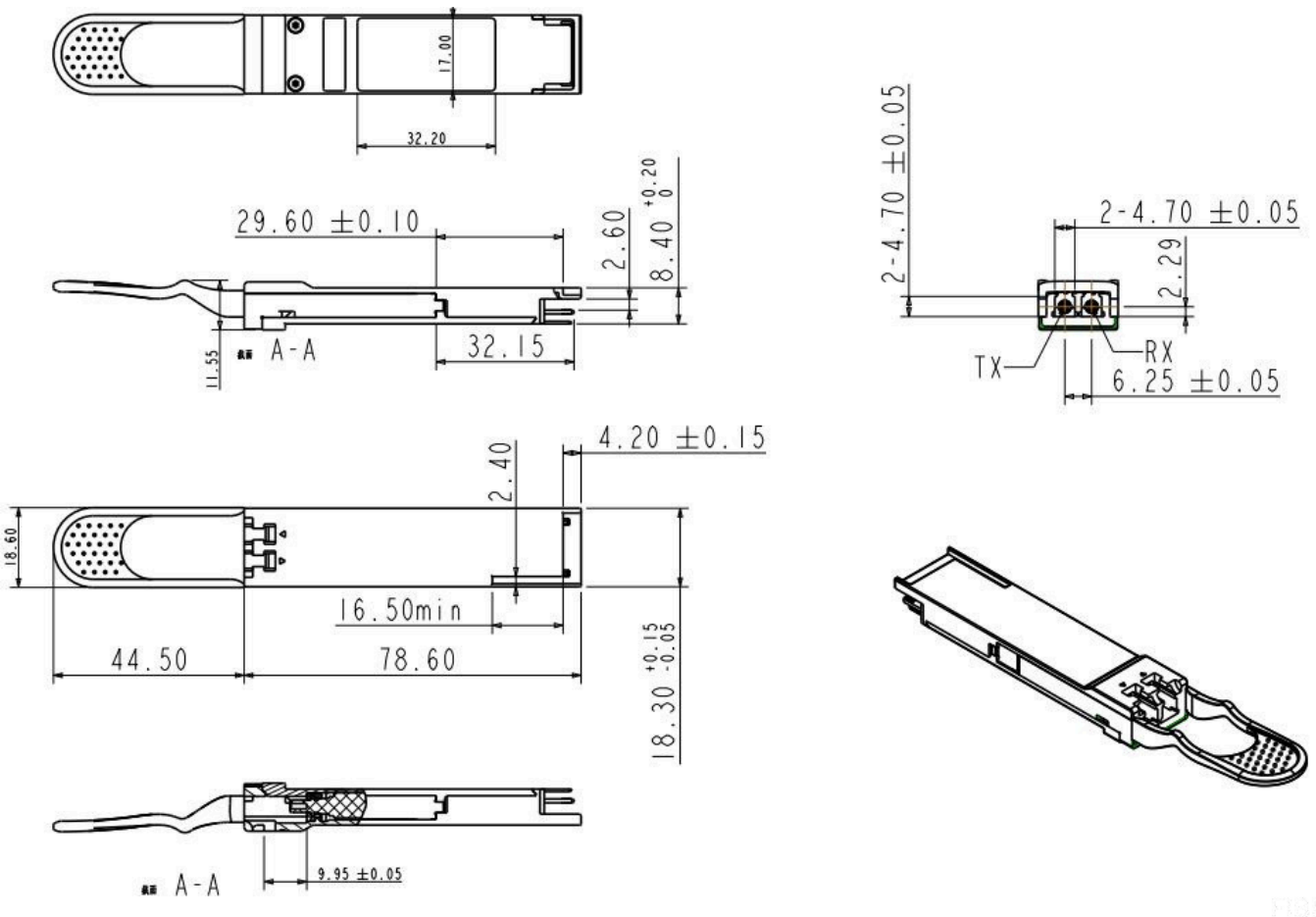
Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
SupplyCurrent	Icc			1.12	A
TransceiverPower-onInitializationTime1				200	ms
Transmitter (each Lane)				0	
Single-endedInputVoltageTolerance		-0.3		4.0	V
ACCommonModeInputVoltageTolerance		15			mV
DifferentialInputVoltage		50			mVp-p
DifferentialInputVoltageSwing	Vin	190		1000	mVp-p
DifferentialInputImpedance	Zin	90	100	110	Ohm
Receiver (each lane)					
Single-endedOutputVoltage		-0.3		4.	V
ACCommonModeOutput				0	mV
DifferentialOutputVoltageSwing	Vout	300		7. 900	mVp-p
DifferentialOutputImpedance	Zout	90	100	5 110	Ohm

Note:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.

Mechanical Dimensions



Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Lane Wavelength	L0	1264.5	1271	1277.5	nm
	L1	1284.5	1291	1297.5	nm
	L2	1304.5	1311	1317.5	nm
	L3	1324.5	1331	1337.5	nm
Transmitter					
SideModeSuppressionRatio	SMSR	30			dB
TotalAverageLaunchPower	PT			8.	dBm
AverageLaunchPower(eachLane)	PAVG	-6.5		5	dBm
OpticalModulationAmplitude1(eachlane)	POMA	-4.0		2.	dBm
LaunchPowerinOMAminusTDP TransmitterandDispersionPenalty(TDP)(eachlane)		-5		5 2.	dB dB
ExtinctionRatio	TDP			3.0 5	dB
RelativeIntensityNoise	ER	3			dB/Hz
OpticalReturnLossTolerance	RIN			-130	dB
TransmitterReflectance	TOL			20	dB
AverageLaunchPowerofOFFtransmitter(eachlane)	RT			-12	dBm
EyeMaskCoordinates2:X1,X2,X3,Y1,Y2,Y3	POFF			-30	
	{0.31,0.4,0.45,0.34,0.38,0.4}				
Receiver					
DamageThreshold3(eachlane)	THd	3.5			dBm
AverageReceivePower(eachlane)		-11.5		2.	dBm
ReceivePower(OMA)(eachlane)				5	dBm
ReceiverSensitivity(OMA)4(eachlane)	SEN			2.	dBm
Stressed Receiver Sensitivity (OMA)5 (each Lane)				5 -7.3	dBm
LOSAssert				-1.	
LOSDe-Assert–OMA			-1	0	dBm
LOSHysteresis			6	-7.5	dBm
ReceiverElectrical3dBupperCutoffFrequency(eachLane)		0.5	-1	2	dB
	Fc		4	31	GHz
Conditions of Stress Receiver Sensitivity Test6					
VerticalEyeClosurePenalty6	VECP		1.9		dB
StressedEyeJ2Jitter	J2		0.33		UI
StressedEyeJ4Jitter	J4		0.48		UI

Note：

1. Even if the TDP <1dB, the OMA min must exceed the minimum value specified here.

2. Hit ratio of 5e-5, per IEEE; See Figure 2 below.

3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this

power level on one lane. The receiver does not have to operate correctly at this input power.

4. Measured with conformance test signal at receiver input for BER = 5e-5 BER.

5. Measured with CWDM4 MSA conformance test signal at TP3 for 5e-5 BER.

6. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

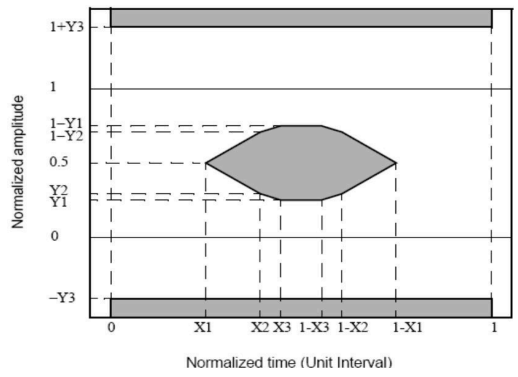


Figure 2. Eye Mask

Pin Description

Pin	Logic	Sym bol	Name/Description
1		GND	Module Ground1 Transmitter
2	CML-I	Tx2-	inverted data input Transmitter non-
3	CML-I	Tx2+	inverted data input Module Ground1
4		GND	Transmitter inverted data input
5		Tx4-	Transmitter non-inverted data input
6	CML-I	Tx4+	Module Ground1 Module Select2
7	CML-I	GND	Module Reset2 +3.3V Receiver
8		MODSEIL	Power Supply 2-wire Serial
9	LVTTL-I	ResetL	interface clock2 2-wire Serial
10	LVTTL-I	VCCRx	interface data2 Module Ground1
11		SCL	Receiver non-inverted data output
12		SDA	Receiver inverted data output
13	LVCMOS-I	GND	Module Ground1 Receiver non-
14	LVCMOS-I/O	RX3+	inverted data output Receiver
15		RX3-	inverted data output Module
16	CML-O	GND	Ground1 Module Ground1 Receiver
17	CML-O	RX1+	inverted data output
18		RX1-	
19		GND	
20	CML-O	GND	
21	CML-O	RX2-	
	CML-O		

Pin	Logic	Symbol	Name/Description
22	CML-O	RX2+	Receivernon-inverteddataoutput
23		GND	ModuleGround1
24	CML-O	RX4-	Receiverinverteddataoutput
25	CML-O	RX4+	Receivernon-inverteddataoutput
26		GND	ModuleGround1
27			ModulePresent,internalpulleddowntoGND
28	LVTTL-O	ModPrsL	Interruptoutput,shouldbepulleduponhostboard2
29	LVTTL-O	IntL	+3.3VTransmitterPowerSupply
30		VCCTx	+3.3VPowerSupply
31		VCC1	LowPowerMode2
32	LVTTL-I	LPMode	ModuleGround1
33			Transmitternon-inverteddatainput
34		GND	Transmitterinverteddatainput
35	CML-I	Tx3+	ModuleGround1
36	CML-I	Tx3-	Transmitternon-inverteddatainput
37		GND	Transmitterinverteddatainput
38	CML-I	Tx1+	ModuleGround1
	CML-I	Tx1-	
		GND	

Note:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

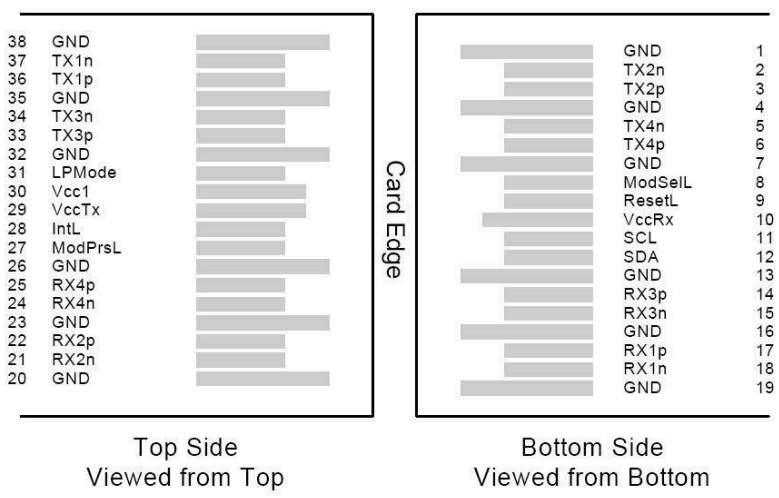


Figure 3. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse

length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

FIBERSTAMP QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

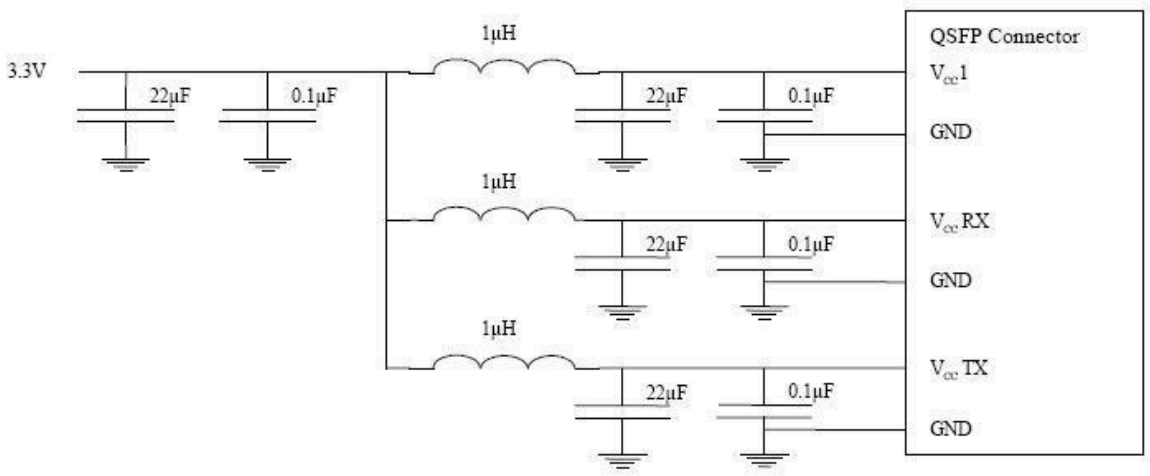


Figure 4. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units
TemperatureMonitorAbsoluteError1	DMI_Temp	-3	3	ºC
SupplyVoltageMonitorAbsoluteError2	DMI_Vcc	-0.1	0.1	V
ChannelRXPowerMonitorAbsoluteError3	DMI_RX_Ch	-2	2	dB
ChannelBiasCurrentMonitor	DMI_Ibias_Ch	-10%	10%	mA
ChannelTXPowerMonitorAbsoluteError3	DMI_TX_Ch	-2	2	dB

Notes:

1. Over operating temperature range.

2. Over full operating range.

3. Due to measurement accuracy of different single mode fibers, there could be an additional ±1dB fluctuation, or a ±3 dB total accuracy.

Digital diagnostics monitoring function is available on all FIBERSTAMP QSFP28 transceivers. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

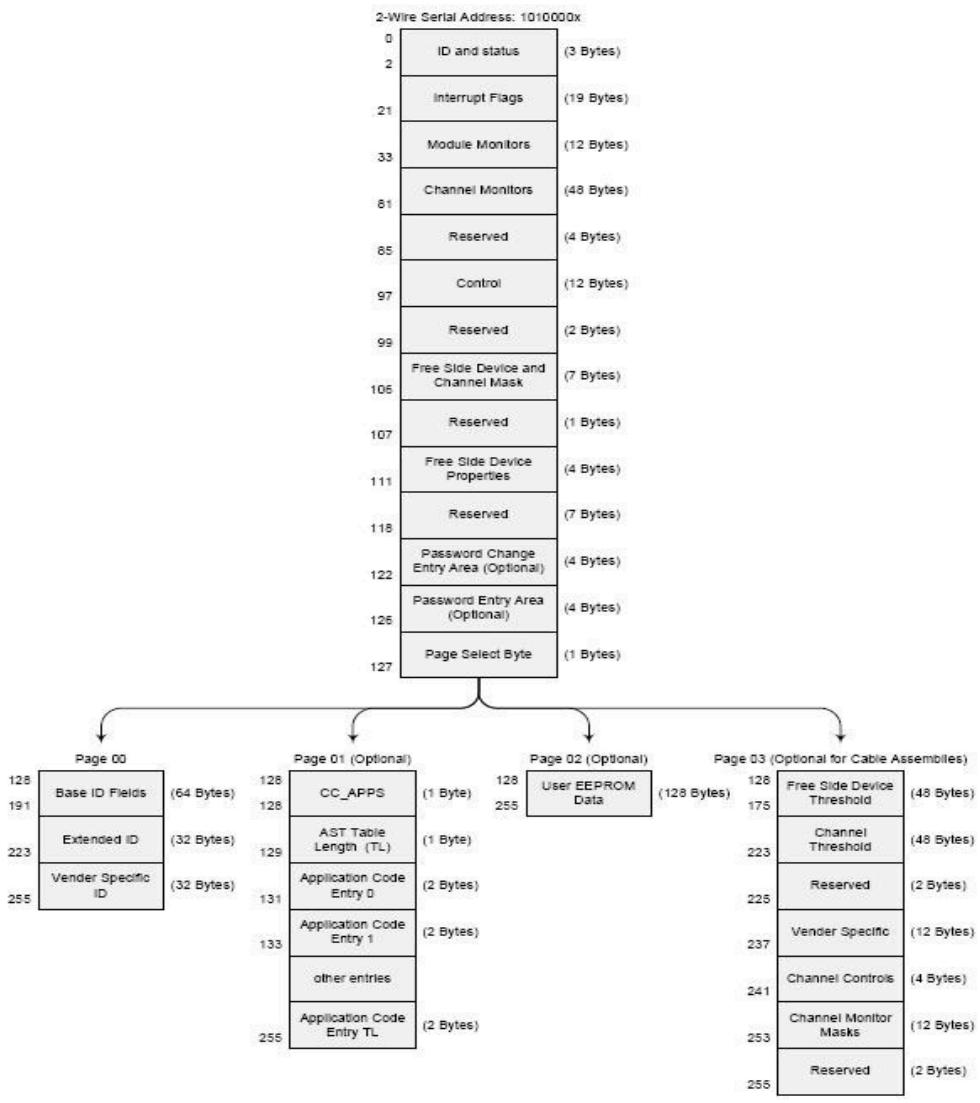


Figure 5. QSFP28 Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure 6. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 7. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand†
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure 8. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and Page 00. Page 03 upper memory please see SFF-8436 document.

SFF-8636 Definiens

TX AND RX CDR LOL indicator (Byte 5)

5	7	L-Tx4 LOL	Latched TX CDR LOL indicator, ch 4	0	0	0	0
	6	L-Tx3 LOL	Latched TX CDR LOL indicator, ch 3	0	0	0	0
	5	L-Tx2 LOL	Latched TX CDR LOL indicator, ch 2	0	0	0	0
	4	L-Tx1 LOL	Latched TX CDR LOL indicator, ch 1	0	0	0	0
	3	L-Rx4 LOL	Latched RX CDR LOL indicator, ch 4	0	0	0	0
	2	L-Rx3 LOL	Latched RX CDR LOL indicator, ch 3	0	0	0	0
	1	L-Rx2 LOL	Latched RX CDR LOL indicator, ch 2	0	0	0	0
	0	L-Rx1 LOL	Latched RX CDR LOL indicator, ch 1	0	0	0	0

TX AND RX CDR BYPASS CONTROL (Byte 98)

98	7	Tx4_CDR_control	Channel 4 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	6	Tx3_CDR_control	Channel 3 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	5	Tx2_CDR_control	Channel 2 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	4	Tx1_CDR_control	Channel 1 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	3	Rx4_CDR_control	Channel 4 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	2	Rx3_CDR_control	Channel 3 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	1	Rx2_CDR_control	Channel 2 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	0	Rx1_CDR_control	Channel 1 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0

TABLE 6-33 OUTPUT DIFFERENTIAL AMPLITUDE CONTROL (PAGE 03H BYTES 238-239)

Value	Receiver Output Amplitude No Output Equalization	
	Nominal	Units
1xxxb	Reserved	
0111b	Reserved	mV(P-P)
0110b	Reserved	mV(P-P)
0101b	Reserved	mV(P-P)
0100b	Reserved	mV(P-P)
0011b	600-1200	mV(P-P)
0010b	400-800	mV(P-P)
0001b	300-600	mV(P-P)
0000b	100-400	mV(P-P)

TABLE 6-34 INPUT EQUALIZATION (PAGE 03H BYTES 234-235)

Value	Transmitter Input Equalization	
	Nominal	Units
11xxb	Reserved	
1011b	Reserved	
1010b	10	dB
1001b	9	dB
1000b	8	dB
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	No EQ

TABLE 6-35 OUTPUT EMPHASIS CONTROL (PAGE 03H BYTES 236-237)

Value	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	Units
1xxxb	Reserved	
0111b	7	dB
0110b	6	dB
0101b	5	dB
0100b	4	dB
0011b	3	dB
0010b	2	dB
0001b	1	dB
0000b	0	No Emphasis

Timing for Soft Control and Status Functions

Parameter	Symbo l	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t _serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t _reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin: LPMode=VIH) until module power consumption enters lower Power Level
IntL Assert Time	t on_Int L	200	ms	Time from occurrence of condition triggering IntL until

				Vout: IntL=VOL
IntLDeassertTime	toff_IntL	500	μs	Time from clear on read3 operation of associated flag untilVout:IntL=VOH.ThisincludesdeasserttimesforRxLOS, Tx Fault and other flag bits.
RxLOSAssertTime	ton_los	10	m	TimefromRxLOSstatetoRxLOSbitsetandIntLasserted
TxFaultAssertTime	ton_Txfault	0	s	TimefromTxFaultstatetoTxFaultbitsetandIntLasserted
FlagAssertTime	ton_flag	20 2000	m ms s	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
MaskAssertTime	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
MaskDeassertTime	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelLAssertTime	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelLDeassertTime	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-rideor Power-setAssertTime	ton_Pdown	100	ms	TimefromP_Downbitset4untilmodulepower consumptionenterslowerPowerLevel
Power_over-rideor Power-setDeassertTime	toff_Pdown	300	ms	TimefromP_Downbitcleared4untilthemoduleisfully functional3

Note：

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value. 2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.

3. Measured from falling clock edge after stop bit of read transaction.

4. Measured from falling clock edge after stop bit of write transaction.